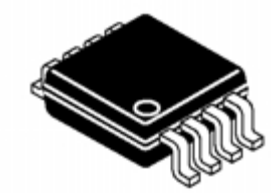
ZXMN2A02X8

20V N-CHANNEL ENHANCEMENT MODE MOSFET

SUMMARY

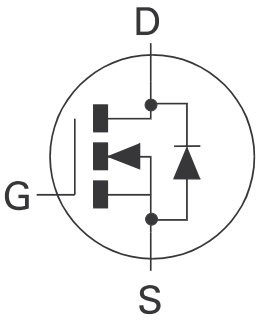
$V_{(BR)DSS}$=20V; $R_{DS(ON)}$=0.02Ω I_D=7.6A



MSOP8

DESCRIPTION

This new generation of TRENCH MOSFETs from Zetex utilizes a unique structure that combines the benefits of low on-resistance with fast switching speed. This makes them ideal for high efficiency, low voltage, power management applications.

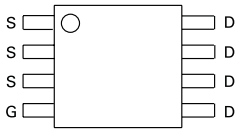


FEATURES

- Low on-resistance
- Fast switching speed
- Low threshold
- Low gate drive
- Low profile SOIC package

APPLICATIONS

- DC - DC Converters
- Power Management Functions
- Disconnect switches
- Motor control



Top View

ORDERING INFORMATION

DEVICE	REEL SIZE	TAPE WIDTH	QUANTITY PER REEL
ZXMN2A02X8TA	7″	12mm	1000 units
ZXMN2A02X8TC	13″	12mm	4000 units

DEVICE MARKING

- ZXMN
  2A02

ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DSS}	20	V
Gate Source Voltage	V_{GS}	±12	V
Continuous Drain Current V_{GS}=10V; T_A=25°C (b) V_{GS}=10V; T_A=70°C (b) V_{GS}=10V; T_A=25°C (a)	I_D	7.6 6.1 6	A
Pulsed Drain Current (c)	I_{DM}	27	A
Continuous Source Current (Body Diode) (b)	I_S	3.1	A
Pulsed Source Current (Body Diode) (c)	I_{SM}	27	A
Power Dissipation at T_A=25°C (a) Linear Derating Factor	P_D	1.1 8.8	W mW/°C
Power Dissipation at T_A=25°C (b) Linear Derating Factor	P_D	1.8 14.4	W mW/°C
Operating and Storage Temperature Range	T_j:T_{stg}	-55 to +150	°C

THERMAL RESISTANCE

PARAMETER	SYMBOL	VALUE	UNIT
Junction to Ambient (a)	$R_{\theta JA}$	113	°C/W
Junction to Ambient (b)	$R_{\theta JA}$	70	°C/W

NOTES

(a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions

(b) For a device surface mounted on FR4 PCB measured at t≤10 secs.

(c) Repetitive rating 25mm x 25mm FR4 PCB, D = 0.05, pulse width 10μs - pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (at T_A = 25°C unless otherwise stated).

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS.
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	20			V	I_D=250μA, V_{GS}=0V
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	V_{DS}=20V, V_{GS}=0V
Gate-Body Leakage	I_{GSS}			100	nA	V_{GS}=±12V, V_{DS}=0V
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.7			V	I_D=250μA, V_{DS}= V_{GS}
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$			0.02 0.04	Ω Ω	V_{GS}=4.5V, I_D=11A V_{GS}=2.5V, I_D=8.4A
Forward Transconductance (1)(3)	g_{fs}		27		S	V_{DS}=10V,I_D=11A
DYNAMIC (3)						
Input Capacitance	C_{iss}		2050		pF	V_{DS}=15 V, V_{GS}=0V, f=1MHz
Output Capacitance	C_{oss}		300		pF	
Reverse Transfer Capacitance	C_{rss}		183		pF	
SWITCHING(2) (3)						
Turn-On Delay Time	$t_{d(on)}$		6.9		ns	V_{DD} =10V, I_D=5.5A R_G=6.0Ω, V_{GS}=5V
Rise Time	t_r		12.2		ns	
Turn-Off Delay Time	$t_{d(off)}$		32.5		ns	
Fall Time	t_f		11		ns	
Total Gate Charge	Q_g		18.6		nC	V_{DS}=10V,V_{GS}=4.5V, I_D=5.5A
Gate-Source Charge	Q_{gs}		4.1		nC	
Gate-Drain Charge	Q_{gd}		5.1		nC	
SOURCE-DRAIN DIODE						
Diode Forward Voltage (1)	V_{SD}		0.8	0.95	V	T_J=25°C, I_S=11A, V_{GS}=0V
Reverse Recovery Time (3)	t_{rr}		19.3		ns	T_J=25°C, I_F=5.5A, di/dt= 100A/μs
Reverse Recovery Charge (3)	Q_{rr}		9.1		nC	

NOTES

(1) Measured under pulsed conditions. Width=300μs. Duty cycle ≤ 2% .

(2) Switching characteristics are independent of operating junction temperature.

(3) For design aid only, not subject to production testing.

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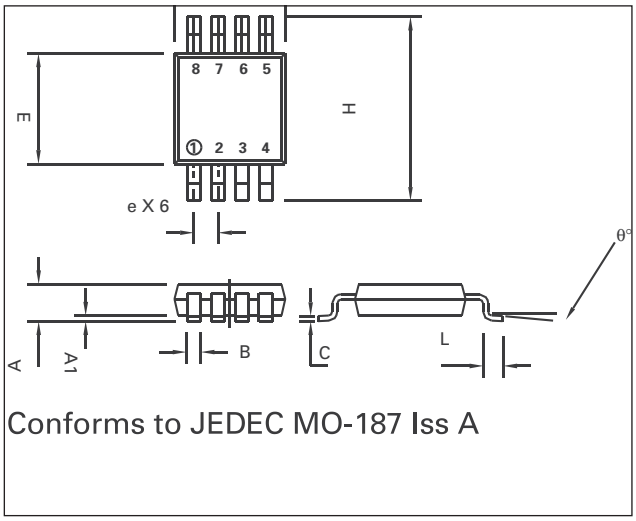
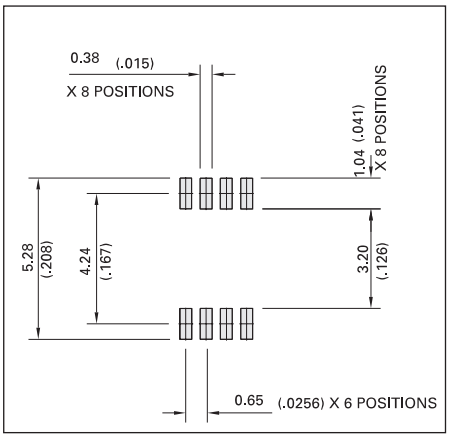
PACKAGE DIMENSIONS



Conforms to JEDEC MO-187 Iss A

DIM	Millimetres		Inches	
	MIN	MAX	MIN	MAX
A		1.10		0.043
A1	0.05	0.15	0.002	0.006
B	0.25	0.40	0.010	0.016
C	0.13	0.23	0.005	0.009
D	2.90	3.10	0.114	0.122
e	0.65	BSC	0.0256	BSC
E	2.90	3.10	0.114	0.122
H	4.90	BSC	0.193	BSC
L	0.40	0.70	0.016	0.028
θ°	0°	6°	0°	6°

PAD LAYOUT DETAILS



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